IN THE CLAIMS

Please cancel claims 1-15 without prejudice, and add new claims 16-23.

1-15 (canceled)

16. (new) A method for executing instructions of a computer program, comprising:

in executing a probe-cache instruction, determining whether data referenced by the probe-cache instruction are present in a cache, without reading the data from the cache in response to the data being present in the cache and without loading the data from memory in response to the data not being present in the cache;

in response to the data being present in the cache, fetching and executing a first instruction that immediately follows the probe-cache instruction in the program code; and

in response to the data not being present in the cache, fetching and executing a second instruction other than the first instruction.

17. (new) The method of claim 16, wherein the second instruction is two instruction addresses after the probe-cache instruction.

18. (new) The method of claim 16, wherein the probe-cache instruction includes a target address, and the second instruction is at the target address.

19. (new) The method of claim 16, wherein the target address specified by the probe-cache instruction references an address of a sub-routine and further comprising returning control to an instruction immediately following the probe-cache instruction in response to completion of the subroutine.

20. (new) An apparatus for executing instructions of a computer program, comprising:

means responsive to execution of a probe-cache instruction, for determining whether data referenced by the probe-cache instruction are present in a cache, without reading the data from the cache in response to the data being present in the cache and without loading the data from memory in response to the data not being present in the cache;

means responsive to the data being present in the cache, for fetching and executing a first instruction that immediately follows the probe-cache instruction in the program code; and

means responsive to the data not being present in the cache, for fetching and executing a second instruction other than the first instruction.

21. (new) A computing arrangement comprising:

a processor configured to execute a program;

a cache memory coupled to the processor;

a system memory coupled to the cache memory;

means coupled to the processor and responsive to execution of a probe-cache instruction by the processor, for determining whether data referenced by the probe-cache instruction are present in a cache, without reading the data from the cache in response to the data being present in the cache and without loading the data from memory in response to the data not being present in the cache;

means responsive to the data being present in the cache, for fetching and executing a first instruction that immediately follows the probe-cache instruction in the program code; and

means responsive to the data not being present in the cache, for fetching and executing a second instruction other than the first instruction.

22. (new) The arrangement of claim 21, wherein the second instruction is two instruction addresses after the probe-cache instruction.

23. (new) The arrangement of claim 32, wherein the probe-cache instruction includes a target address, and the second instruction is at the target address.

23. (new) The arrangement of claim 21, wherein the target address specified by the probe-cache instruction references an address of a sub-routine and further comprising means for returning control to an instruction immediately following the probe-cache instruction in response to completion of the subroutine.